**MAWLANA BHASHANI SCIENCE AND TECHNOLOGY UNIVERSITY**

SANTOSH, TANGAIL-1902



DEPARTMENT OF INFORMATION AND COMMUNICATION TECHNOLOGY

**Course Title: Digital Logic Design Lab**

**Course Code: ICT-2104**

**Lab Report on:** Verification of AND, OR, and NOT Gates

**Lab Report No: 01**

|  |  |
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| Submitted By | Submitted To |
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**Date of Performance:**

**Date of Submission:**

**Experiment No:** 1

**Experiment Name:** Verification of AND, OR, and NOT Gates

**Objective:** The objective of this experiment is to verify the truth tables of basic logic gates (AND, OR, NOT) and confirm their functionality by implementing their circuits using ICs.

**Materials Required:**

* Breadboard
* Power supply (5V DC)
* Connecting wires
* IC 7408 (AND Gate)
* IC 7432 (OR Gate)
* IC 7404 (NOT Gate)
* LEDs (to display outputs)
* Resistors (220Ω for limiting current)
* Multimeter (optional)

**Procedure:**

**1. AND Gate (IC 7408):**

- Place IC 7408 on the breadboard.

- Connect pin 7 to ground and pin 14 to +5V to power the IC.

- Use pin 1 and pin 2 as inputs, and connect pin 3 as the output.

- Apply different combinations of inputs (0V for logic 0, and 5V for logic 1) to the gate and observe the output on an LED connected to pin 3.

**2. OR Gate (IC 7432):**

- Insert IC 7432 on the breadboard.

- Connect pin 7 to ground and pin 14 to +5V.

- Pin 1 and pin 2 are the input pins, while pin 3 is the output pin.

- Connect the inputs and record the outputs for all possible combinations.

**3. NOT Gate (IC 7404):**

- Place IC 7404 on the breadboard.

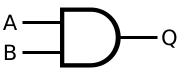
- Connect pin 7 to the ground and pin 14 to +5V.

- Pin 1 is the input, and pin 2 is the output for the NOT gate.

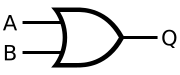
- Test the output by giving the input either a logic 0 (0V) or a logic 1 (5V).

**Diagrams:**

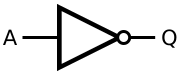
**1. AND Gate Symbol:**



**2. OR Gate Symbol:**



3. NOT Gate Symbol:



**Truth Tables:**

**1. AND Gate:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Q (A AND B)** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

2. OR Gate:

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Q (A OR B)** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

3. NOT Gate:

|  |  |
| --- | --- |
| **A** | **Q (A’)** |
| 0 | 1 |
| 1 | 0 |

**Discussion:**

In this experiment, we have successfully verified the functionality of the AND, OR, and NOT gates by constructing their circuits and observing their outputs concerning the truth tables.